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Design and Analysis of Phase Locked Loop Based Frequency Synthesizer Using Source Coupled VCO: A Review

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Abstract: The CMOS PLL based Frequency Synthesizer is a vital role in Receiver front end Sub component. The main objective of this paper is to design a high frequency of oscillation, less phase noise and power efficient PLL. In general, the PLL contains PFD, Loop Filter, VCO and Frequency Divider, Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. Here the Source Coupled VCO is proposed with adaptive voltage level technique. It is designed in Tanner tool.

Keywords: Source Coupled VCO, PFD, PLL, Tanner tool, Frequency Divider and Charge Pump.

I. INTRODUCTION

A PLL is a feedback system that compares the output frequency/phase with the input frequency/phase. Phase-locked loops can be making used for frequency synthesizing, carrier synchronization, carrier recovery, frequency division, frequency multiplication and frequency Demodulation. A VCO is the compassion of the PLL and can be designed either by LC or RC. A LC VCOs have higher phase noise performance compared with ring VCO'S. Nevertheless, the LC VCO has a small tuning range for large layout area and probably has higher power. The ring oscillators do not have the problem of the on-chip inductors vital for the LC oscillators.

Hence, the chip area is reduced. The phase noise performance of ring oscillators is much poorer in general. In addition, by the side of high oscillation frequencies, the power consumption of the ring oscillators possibly will not be low which is a key requirement for battery-operated devices. To resolve these complications, we put effort on single stage source coupled VCO exclusive of using an LC tank circuit. Current work is done with major intention of reduced power consumption in design of VCO with different reduction techniques. The main part of this PLL is the SCVCO, which has been designed to get superior phase noise.

A. SYSTEM OVERVIEW

The Phase-locked loops (PLLs) generate timely on-chip clocks for different applications such as clock and data recovery, microprocessor clock generation and frequency synthesizer. A PLL is a closed-loop feedback system set predetermined phase correlation between its output clock phase and the phase of a reference clock. A PLL follow the phase changes that are within the bandwidth of the PLL. A PLL is a negative feedback control system circuit. As the name means, the intention of a PLL is to generate a signal during which the phase is same compared to the phase of a reference signal. This is prepared subsequent to many iterations of comparing the reference and feedback signals. Overall target of the PLL is to match the phase of the reference and feedback signals during the lock mode during which PLL output is constant. Afterwards, the PLL prolongs to compare the two signals. A basic form of a PLL consists of four main blocks:

1. Phase Frequency Detector (PFD)
2. Low Pass Filter (LPF)
3. Voltage Controlled Oscillator (VCO)
4. Frequency divider (or) Programmable Counter (÷N)

B. PLL ARCHITECTURE

To synchronize the frequency, different types of PLLs are being used in the application of wireless communication. PLLs are contains of PFD, CP, LPF, SCVCO and frequency divider. This is shown in Fig. 1. In addition to SCVCO and PFD compares feedback signal through input signal and generates the error signal. A charge pump circuit is next to the LPF is used to minimize the conflicts at the input of SCVCO and to get a sharper and flat signal at the SCVCO output. To shape a phase-locked loop (PLL) and the phase error output of PFD is provided to a charge pump. Then the low pass filter mixes the signal to acquire a sharper and smooth signal. Therefore, the conflicts at the input of SCVCO get diminished.

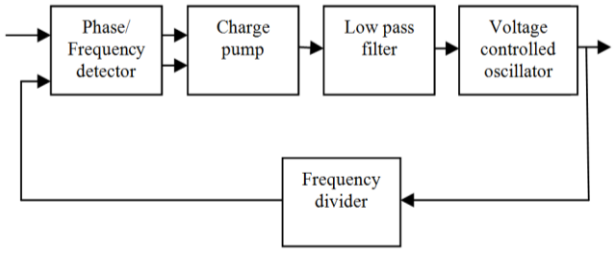

Fig.1.The block diagram of PLL

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II. LITERATURE SURVEY

Literature survey enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

Amit Tripathi , Dr. Rajesh Nema presented a paper entitled as "A Low Power Consumption Single Stage Source Coupled CMOS Voltage Controlled Oscillator (VCO) Using 0.18 µm CMOS Technology ",[1]. This investigation resulted in a single stage CMOS Voltage controlled oscillator with a high oscillation frequency and low power consumption. The VCO is a single stage circuit has a low phase noise due to reduced noise sources.

Table 1: Comparison of results between other VCO and Proposed VCO

Parameter	[1]	[3]	[4]	[9]	Proposed work
Supply Voltage(V)	2.5	2.2	3.3	1.8	1.8
Power Consumption (mW)	15.5	7.01	24.5	4.8	0.72
Tunning Range(GHz)	0.66-1.27	0.2-2.1	0.45-1.15	4.65-5.89	0.58-2.79
No. of stage	2	2	2	1	1
Gate length(um)	0.5	0.35	0.35	0.18	0.18

Arpit Patel, Rakesh Chaudhari , Sarman K. Hadia, Nilesh D.Patel, presented "Wide-Band Current Starved Ring CMOS Voltage Controlled Oscillator (VCO) using 0.18 µm CMOS Technology" This paper describes a design and implementation of Current Starved CMOS Voltage Controlled Oscillator based on Ring Oscillator. Efforts are made to design a CMOS Voltage controlled oscillator having wide frequency range with High frequency, Low power. So, the CMOS VCO designed here having a Five Stage Current Starved CMOS VCO and Seven Stage Current Starved CMOS VCO [2].

Table 2: Comparison of results between five and seven stage current starved VCO.

Parameter	Reference	5-stage CS VCO	7-stage CS VCO
Technology	0.18um	0.18um	0.18um
Supply Voltage(V)	1.8	1.8	1.8
I/P tuning Range(V)	0.1 to 1.8	0.5 to 1.8	0.5 to 1.8
Range of oscillating frequency(MHz)	129.03 to 222.53	18.724 to 1890.4	68.971 to 2099.5
Power Consumption(uW)	58.47	35.39 to 25.013	2.59 to 348.81

Rashmi K Patil, Vrushali G Nasre, This paper describes a performance comparison of two Voltage Controlled oscillator for Phase Locked Loop. "A Performance Comparison of Current Starved VCO and Source Coupled VCO for PLL in 0.18µm CMOS Process", [3]. Current Starved VCO and Source Coupled VCO for PLLs in a 0.18 µm digital CMOS process are designed and their Performances are compared based on high oscillation frequency, low power consumption, and low area. The measurement results show that in chip area, power consumption, a RC based Current starved VCO is superior to a Source Coupled VCO.

Table 3: Measured Performances

Parameter	Current starved VCO	Source coupled VCO
Technology(um)	0.18	0.18
I/P tuning range(V)	0-1.8	1.4-1.9
Range of oscillation frequency(MHz)	25.70 - 222.53	307.69 – 427.35
Area($um^{2)}$	9.68	75.9
Power consumption(mW)	0.1052	6.69

The paper entitled as "Comparative Analyses of Phase Noise in 28nm CMOS LC Oscillator Circuit Topologies: Hartley, Colpitts, and Common-Source Cross-Coupled Differential Pair"[4], presented by **Ilias Chlis, Domenico Pepe and Domenico Zito.** This paper reports comparative analyses of phase noise in Hartley, Colpitts, and common-source cross-coupled differential pair LC oscillator topologies in 28 nm CMOS technology. The impulse sensitivity function is used to carry out both qualitative and quantitative analyses of the phase noise exhibited by each circuit component in each circuit topology with oscillation frequency ranging from 1 to 100 GHz. The comparative analysis show the existence of four distinct frequency regions in which the three oscillator topologies rank unevenly in terms of best phase noise performance, due to the combined effects of device noise and circuit node sensitivity.

K. Gnana Deepika, K. Mariya Priyadarshini and K. David Solomon Raj, designed Sleepy Keeper Approach for Power Performance Tuning in VLSI Design. In this paper sleepy keeper approach is introduced to reduce the power dissipation of the circuit in idle state when its logic is not needed. The sleepy keeper approach uses traditional sleep transistors and two additional transistors which are driven by already calculated gate output. This saves the state during sleep mode. Multi threshold transistors are used in order to reduce subthreshold leakage power and also to increase the switching speed of the circuit [5].

M. Sai Sarath Kumar, M. Aarthy, This work describes a two-stage CMOS Voltage Ring Oscillator (VCRO) using differential delay cells are analyzed. The main aim of the paper is to increase the tuning range of the circuit and obtain a good phase noise at the cost of design complexity and power consumption. [6].

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Table 4: Comparison of Results

Design	[1]	[2]	Present work
Technology	0.18um	0.5um	90nm
Output frequency (GHz)	0.737~ 1.456	0.660~ 1.270	1.413~ 3.03
Tuning range (%)	49.4	48	53.40
Power dissipation (mW)	14.8	15.5	9.02
Phase noise	-103.3	-106	-156.328
Supply voltage (Volt)	2.0	2.5	1.5
No. of stages	2	2	2

Mr.Om Prakash, Dr.B.S.Rai, Dr.Arun Kumar, presented a Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage over static CMOS logic circuits. Dynamic CMOS Circuits, featuring a high speed operation are used in high performance VLSI designs. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power Consumption. In this work, domino gate is designed with various body biasing and high performance circuit was specified [7]. In this paper the designed Domino NAND gate and body bias NAND gate Simulation results shows that the proposed circuit technique consumes less dynamic as well as static power than other techniques. The other benefit of proposed technique is its high noise immunity as compare to other technique.

Rupesh Kumar Patlani, Rekha Yadav, presented a paper in which a complementary metal–oxide–semiconductor (CMOS) ring oscillators and LC VCO and is brief study of high performance VCO on 45 nm technology to achieve the desired objectives such as both non linear and linear operations,"Design of Low Power Ring VCO and LC-VCO using 45 nm Technology", [8]. The Ring VCO consumes less power than the LC-VCO. In Ring VCO, we achieve high oscillation at output. In the estimated design of VCO, main focus is given on power consumption an output frequency.

Table 5: Comparison result of ring VCO and LC-VCO

Parameter	Ring VCO	LC-VCO
Technology	45NM	45NM
Operating voltage	1V	1.1V
Output frequency	11GHz	77GHz
Power consumption	11.64uW	39.55uW

Sheetal Soni, Shyam Akashe, designed a "Noise Sensitivity Analysis of 5 Stages Voltage Controlled Ring Oscillator at nm Technology", [9]. In present paper, design of differential ring oscillator using replica bias circuit has been presented. Qualitative analysis of jitter and phase noise of differential ring oscillators in the time and frequency domain is presented respectively which shows great results for the design issues of voltage controlled ring oscillator. The effect of the different number of transistors and their symmetrical arrangement to phase noise and jitter is analyzed. Good agreement between qualitative and quantitative measurements is observed.

Table 6: Noise sensitivity analysis of Ring VCO at varying frequency

Frequency	Output Noise(uV/sqrt(Hz))	Pnoise(db/Hz)
0.4Hz	31.75	7.963
6.954Hz	7.942	20.69
10.00	6.354	23.72
15.00	5.126	24.58
20.00	5.124	25.111

Table 7: Jitter analysis of Ring Oscillator in time domain

	Frequency (MHz)	Jitter (ns)
Delay cell	1.231	2.413
	1.867	3.113
	1.964	3.557
	2.044	9.363

III. APPLICATIONS

1) Amit Tripathi , Dr. Rajesh Nema designed a Single Stage Source Coupled CMOS Voltage Controlled Oscillator. The oscillator can be used for low-voltage and low-power applications because of its high frequency of oscillation and low power consumption by adaptive voltage technique [1].
2) Rashmi K Patil and Vrushali G Nasre designed two types of VCO. They compare their results and the techniques proposed in this paper can also be applied to other low voltage analog and RF circuits to improve their performance [3].
3) Sheetal Soni and Shyam Akashe presented Noise Sensitivity Analysis of 5 Stages Voltage Controlled Ring Oscillator this help in qualitative analysis of jitter and phase noise of differential ring oscillators in the time and frequency domain and the effect of the different number of transistors and their symmetrical arrangement to phase noise and jitter is analyzed [9].

IV. CONCLUSION

Table 8: Comparison table

Parameter	5-Stage CSVCO	7- Stage CSVCO	Source coupled VCO
Technology (um)	0.18	0.18	0.18
I/P tuning range(V)	0.5 to 1.8	0.5 to 1.8	1.4-1.9
Range of oscillation frequency	18.724 to 1890.4	68.971 to 2099.5	307.69 – 427.35
Power consumption	35.39 to 25.013	2.59 to 348.81	6.69

Modern wireless communication systems require phase locked loop (PLL) mainly on synchronization clock synthesis, skew and jitter reduction. As to increase of speed of the circuit operation, there is required of a PLL circuit with faster locking capability. While increasing the number of stages for getting the higher frequency the power dissipation and size of oscillator was going to increase. Therefore, instead of increasing the number of stages and time constant again control voltage and width of the CMOS can be adjusted for getting the higher frequency.

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